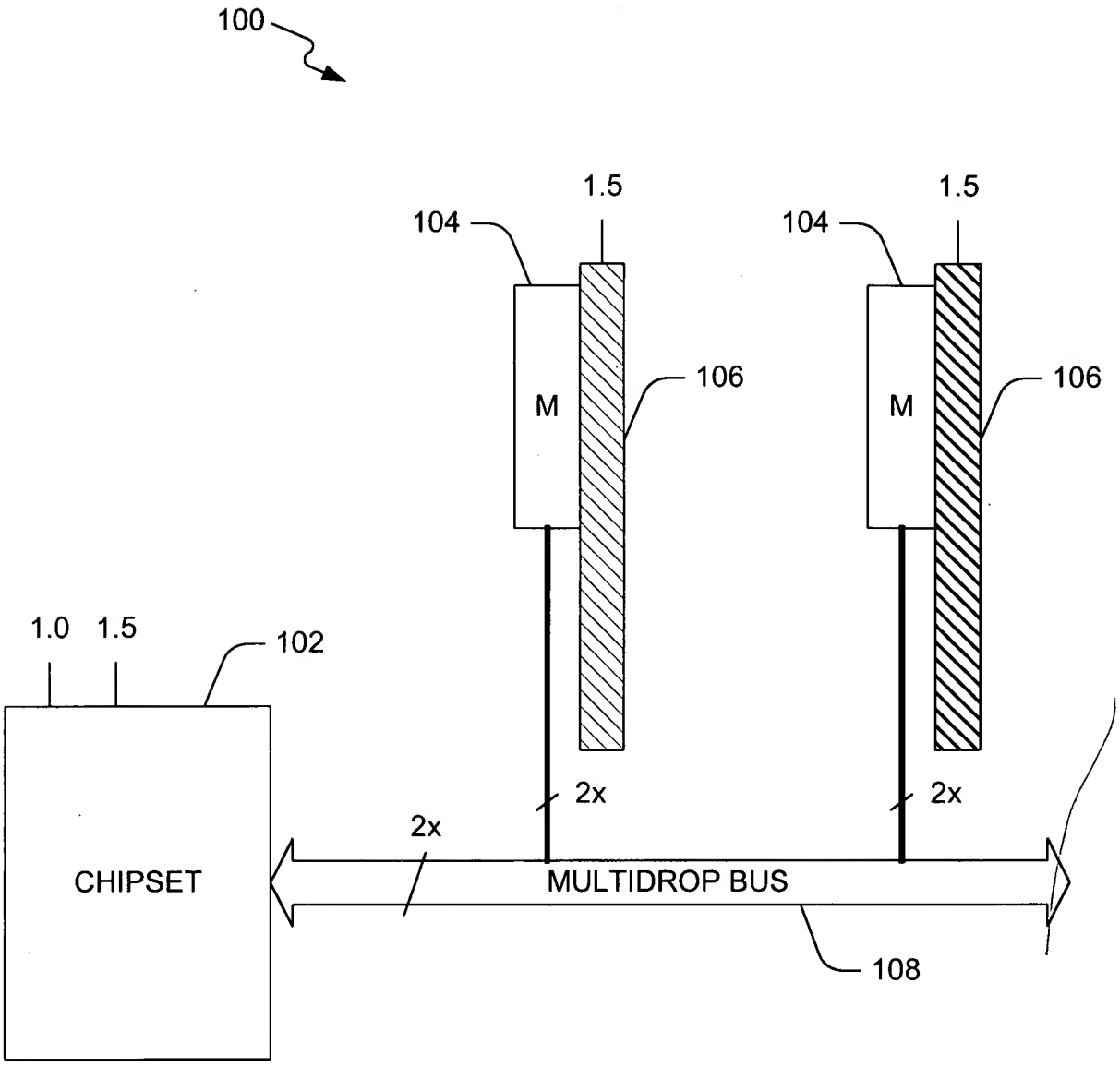

FIG. 1
(PRIOR ART)

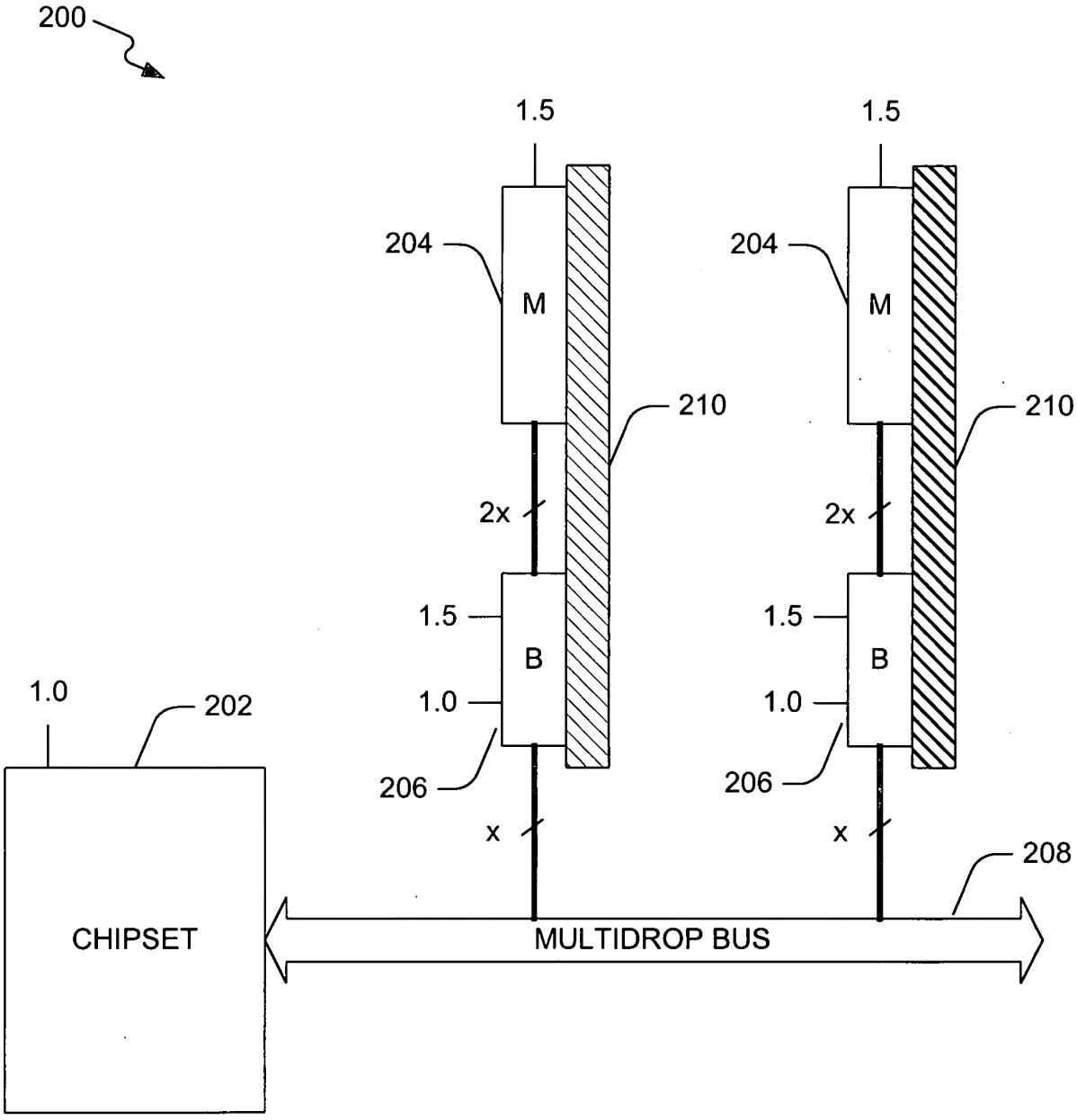
200
1.5
1.5
204
M
204
M
210
210
2x
2x
1.5
B
1.5
B
1.0
1.0
206
206
x
x
208
1.0
202
CHIPSET
MULTIDROP BUS

FIG. 2

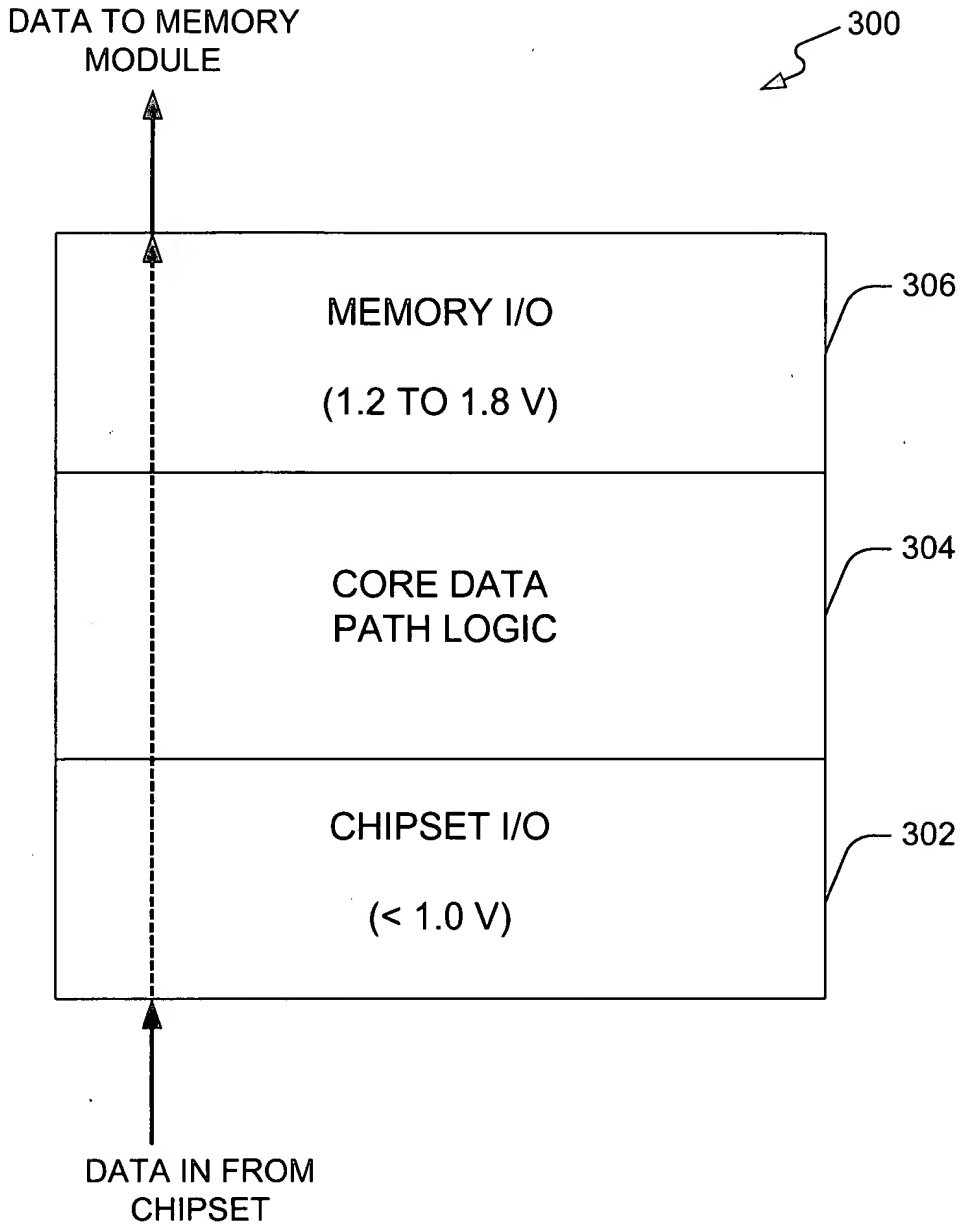
DATA TO MEMORY MODULE
300
MEMORY I/O
(1.2 TO 1.8 V)
306
CORE DATA PATH LOGIC
304
CHIPSET I/O
(< 1.0 V)
302
DATA IN FROM CHIPSET

FIG. 3

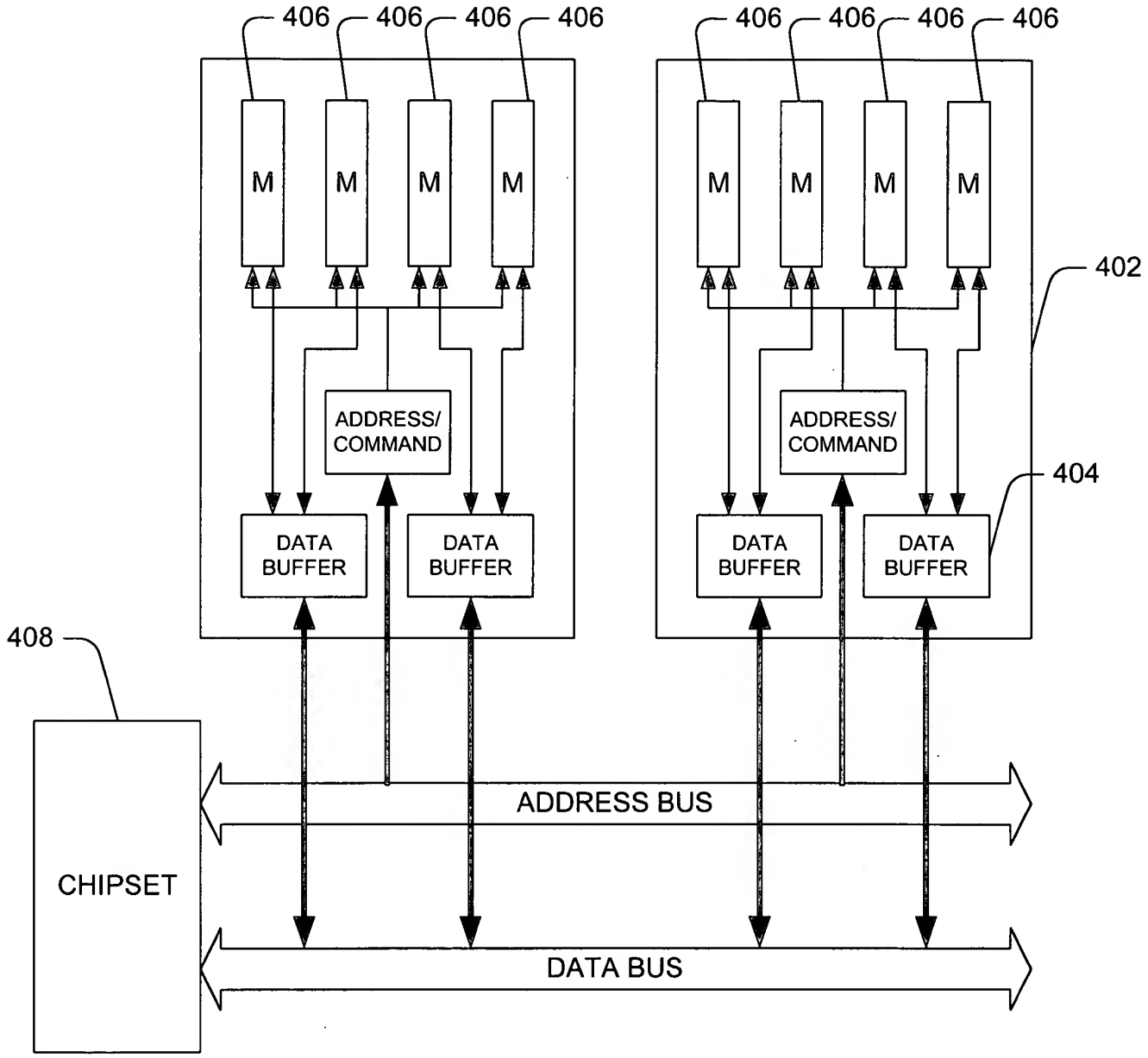
406
406
406
406
406
406
406
406
M
M
M
M
M
M
M
M
402
ADDRESS/
COMMAND
ADDRESS/
COMMAND
404
DATA
BUFFER
DATA
BUFFER
DATA
BUFFER
DATA
BUFFER
408
ADDRESS BUS
CHIPSET
DATA BUS

FIG. 4

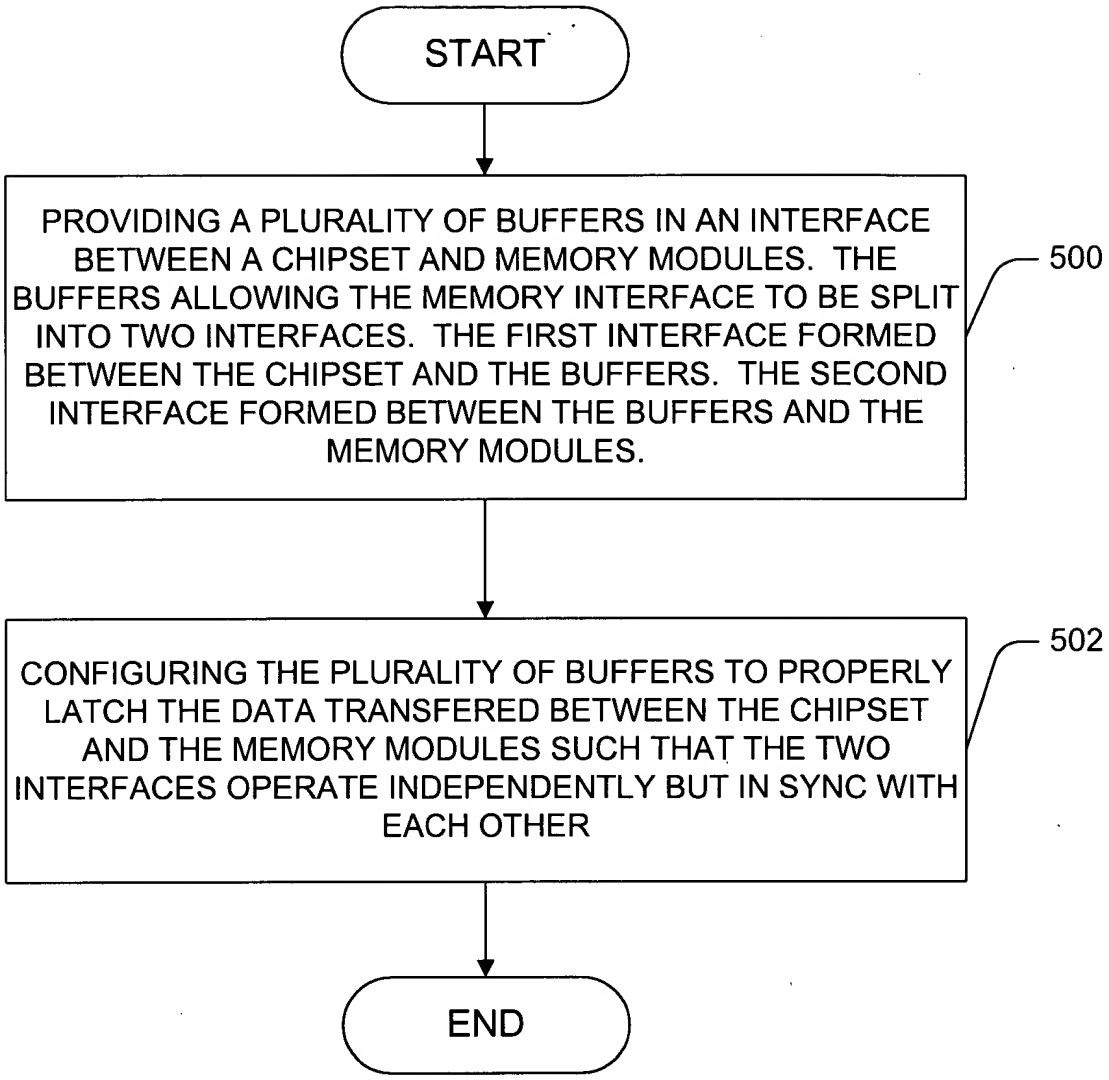
START
PROVIDING A PLURALITY OF BUFFERS IN AN INTERFACE BETWEEN A CHIPSET AND MEMORY MODULES. THE BUFFERS ALLOWING THE MEMORY INTERFACE TO BE SPLIT INTO TWO INTERFACES. THE FIRST INTERFACE FORMED BETWEEN THE CHIPSET AND THE BUFFERS. THE SECOND INTERFACE FORMED BETWEEN THE BUFFERS AND THE MEMORY MODULES.
500
CONFIGURING THE PLURALITY OF BUFFERS TO PROPERLY LATCH THE DATA TRANSFERED BETWEEN THE CHIPSET AND THE MEMORY MODULES SUCH THAT THE TWO INTERFACES OPERATE INDEPENDENTLY BUT IN SYNC WITH EACH OTHER
502
END

FIG. 5